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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,570	08/01/2003	Jhon-Jhy Liaw	TSM03-0196	6324

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SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER	
VINH, LAN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,570	LIAW, JHON-JHY	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948).
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities: It is unclear what it means by "leaving substantially unetched the active layer". Appropriate correction is required. For the purpose of examination, "leaving substantially unetched the active layer" is best understood by the examiner as leaving substantially unetched active layer

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-10, 14, 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Mirbedini et al (US 6,864,152)

Mirbedini discloses a method of fabricating trenches. The method comprises the steps of:

applying a mask layer 202 to an active layer 200 (col 48-49, fig. 2D)

patterning the mask layer to expose areas of the active layer (fig. 2D)

etching the exposed areas of the active layer to form trenches (col 7, lines 11-14)

oxidizing exposed areas of the trench sidewall/active layer (col 7, lines 18-22)

Regarding claim 2, Mirbedini discloses the active layer is an active layer of a silicon-on-insulator wafer (col 5, lines 43-45)

Regarding claim 3, Mirbedini disclose the step of etching includes partially removing the active layer of the exposed areas (fig. 2F)

The method of claim 1 wherein the active layer is about 200 A to about 1000 A in thickness and the step of etcbing includes partially removing the active layer in the exposed areas

Regarding claim 5, Mirbedini discloses that the layer 202/mask layer is about 50-500 Angstroms (col 5, lines 50-52)

Regarding claim 6, fig. 2E shows unetched portion of layer 200/active layer after etching

Regarding claim 8, Mirbedini discloses that the mask layer comprises oxide (col 5, lines 48-49)

Regarding claim 9, Mitbedini discloses the step of removing the layer 202/mask on the active layer after partially removing the active layer in the exposed areas (fig. 2G)

Regarding claim 10, Mitbedini discloses the active layer is formed of silicon (col 5, lines 48-49)

Regarding claims 14-15, Mitbedini discloses that the step of oxidizing in oxygen to create an oxidation layer about 50-500 angstroms (col 7, lines 22-24)

4. Claims 16, 18-20, 22, 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Mirbedini et al (US 6,864,152)

Mirbedini discloses a method of fabricating trenches. The method comprises the steps of:

applying a mask layer 202 to a SOI wafer, the SOI having an active layer 200, an insulator 203 and a substrate (col 48- 49, fig. 2D)

patterning the mask layer to expose areas of the active layer (fig. 2D)

etching the exposed areas of the active layer to form trenches and partially remove the exposed area (col 7, lines 11-14)

oxidizing exposed areas of the trench sidewall/active layer to form oxide liner (col 7, lines 18-22)

Regarding claim 18, Mirbedini discloses using a photoresist during patterning (col 5, lines 60-61)

Regarding claim 19, Mirbedini discloses that the mask layer comprises oxide (col 5, lines 48-49)

Regarding claim 20, Mirbedini discloses that the layer 202/mask layer is about 50-500 Angstroms and a nitride layer (300 –10,000 angstroms (col 5, lines 50-58)

Regarding claims 22, 27, Mitbedini discloses the step of oxidizing in oxygen to create an oxidation layer about 50-500 angstroms (col 7, lines 22-24)

Regarding claims 24-25, Mirbedini discloses the step of removing the layer 202/mask on the active layer 200 (silicon) after partially removing the active layer in the exposed areas (fig. 2G)

Regarding claim 26, fig. 2 E shows some inexposed/inactive areas of the active layer having a thickness remains

5. Claims 28-31, 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Mirbedini et al (US 6,864,152)

Mirbedini discloses a method of fabricating trenches. The method comprises the steps of:

applying a mask layer 202 to a SOI wafer, the SOI having an active layer 200, an insulator 203 and a substrate (col 48- 49, fig. 2D)

patterning the mask layer to form active regions (regions underneath the mask) and inactive regions (fig. 2D)

etching the wafer to form trenches and remove the exposed/inactive regions and substantially most of the active regions remains (col 7, lines 11-14; fig. 2E)

oxidizing exposed areas of the trench sidewall/inactive regions of the active layer to form oxide liner (col 7, lines 18-22)

Regarding claims 29, 34, Mirbedini discloses using a photoresist during patterning (col 5, lines 60-61)

Regarding claim 30, Mirbedini discloses that the mask layer comprises oxide (col 5, lines 48-49)

Regarding claim 31, Mirbedini discloses that the layer 202/mask layer is about 50-500 Angstroms and a nitride layer (300 –10,000 angstroms (col 5, lines 50-58)

Regarding claims 33, 37, Mitbedini discloses the step of oxidizing in oxygen to create an oxidation layer about 50-500 angstroms (col 7, lines 22-24)

Regarding claims 35, 36, Mirbedini discloses the step of removing the layer 202/mask on the active layer 200 (silicon) after partially removing the active layer in the

exposed areas (fig. 2G)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 7, 17, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirbedini et al (US 6,864,152) in view of Yagishita et al (US 6,879,001)

Mirbedini method has been described above. Unlike the instant claimed inventions as per claims 4, 7, 17, 32, Mirbedini fails to disclose that the active layer is about 200-1000 angstroms

Yagishita discloses a method for manufacturing a semiconductor device comprises the step of forming an active layer having a thickness of 30 nm/300 angstroms or 10 nm/100 angstroms or smaller (col 7, lines 14-24)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Mirbedini method by forming an active layer having the thickness as per Yagishita to increase the threshold voltage value of the transistor (col 7, lines 17-21)

8. Claims 11-13, 21, 23, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mirbedini et al (US 6,864,152) in view of Yamauchi (US 6,642,124)

Mirbedini method has been described above. Unlike the instant claimed inventions

as per claims 11-13, 21, 23, 38, Mirbedini fails to disclose performing the oxidizing step RTA (rapid thermal anneal) at a temperature of 500-1250^0 C

Yamauchi discloses a method for manufacturing a semiconductor device comprises the step of performing an oxidizing step by RTA (rapid thermal anneal) at a temperature of 1050-1150^0 C (col 5, lines 16-20)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Mirbedini method by performing an oxidizing step by RTA (rapid thermal anneal) at a temperature of 1050-1150^0 C as per Yamauchi because Yamauchi discloses that oxidizing is performed by first implementation oxidation in an oxygen atmosphere at 1050-1150^0 C (col 5, lines 15-18)

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
May 9, 2005